FPGA Simulation of AD Converter by using Giga Hertz Speed Data Acquisition for Partial Discharge Detection

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***Abstract*-** Currently, FPGA (Field Programmable Gate Array) technology is being widely used for accelerator control owing to its fast digital processing capability.This paper is purely a model to determine the design circuit to implement Partial Discharge (PD) detection in FPGA technology. The research shall involve ISE Simulator version 9.2i (Xilinx) and Very high integrated circuit Hardware Description Language (VHDL) programming to evaluate the use of Field Programming Gate Array (FPGA) for the detection and counting of partial discharge signals in underground cable. The impulse signals at the input data have very fast rise time in the range of 1 ns to 2 ns.

***Keyword*-** Partial Discharge Detection, FPGA Simulation, FPGA Technology, ADC with Peak Detector Block, Real Time Processing, Underground Cable, Counter with Reset Block, VHDL Programming.

I. INTRODUCTION

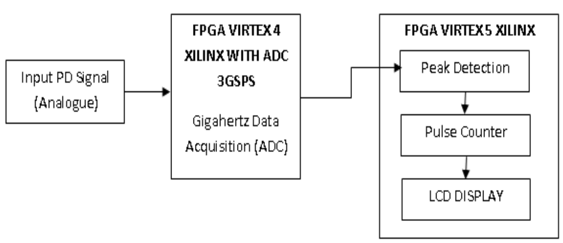


Fig. 1 Block Diagram Partial Discharge Detection using Gigahertz Data Acquisition with FPGA Technology

FPGA compiler use (Test Bench) Xilinx ISE simulator and Xilinx Synthesis Technology (XST) to process synthesis and simulate real time data from output Analogue to Digital Converter (ADC) block to Peak Detection Block, and then process counting PD signal in Impulse Counter with Reset Block (30 bit). The impulse PD signals at the input data have very fast rise time in the range of 1 ns to 2 ns. Fig.1 shows the typical block diagram for detecting and monitoring partial discharge signal.

PD detection system is an automatic system that can detect and display PD signals from underground cable for easy readout. PD detection system can work without oscilloscope, computer or any other associated costly measuring equipment. PD signal is detected by using magnetic probe sensor. This system can detect the PD signal in underground cable from above the ground without outage.

A Partial Discharge (PD) is a flow of electrons and ions which occurs in a gas over a small volume of the total insulation system. This short duration series of events or impulse emit acoustic, optical, electrical and electromagnetic energy. PDs can be detected by measuring any of this radiation energy.[1]

The work in this paper primarily involved modeling, which comprises a FPGA compiler ISE Xilinx Synthesize Technology (XST) and ISE Xilinx simulator approach whereby the impulse signals will be processed, detected and counted using ADC with peak detector block and counter with reset block. In the next stage, this method will be implemented on a lab simulation scale for testing and validation. With this method of PD detection, real PD signals can be detected although the PD signals from magnetic probe sensor are too weak. The PD signals can also be counted and displayed clearly even if the PD signals have too much distortion.

The functional approach of the ADC with peak detector block and counter with reset block will be dealt in this paper. The physics of PD generation and data acquisition system are very extensive and broad. Thus, they are not dealt in this work.

In short a PD gives rise to voltage and current pulses with time durations in the range of a few nanosecond (ns), travelling at velocity of electromagnetic waves. Due to the high sensitivity of magnetic probes, the shape of the pulse is preserved with very high integrity.

II. DESIGN BLOCK OF THE PD DETECTION

Fig. 2 shows the functional approach of the ADC with peak detector block and impulse counter with reset block in the overall processing layout to count the PD signals. Other blocks such as latch data block, reset automatic block and driver LCD block are not dealt in this work.

A. Block ADC and Peak Detector

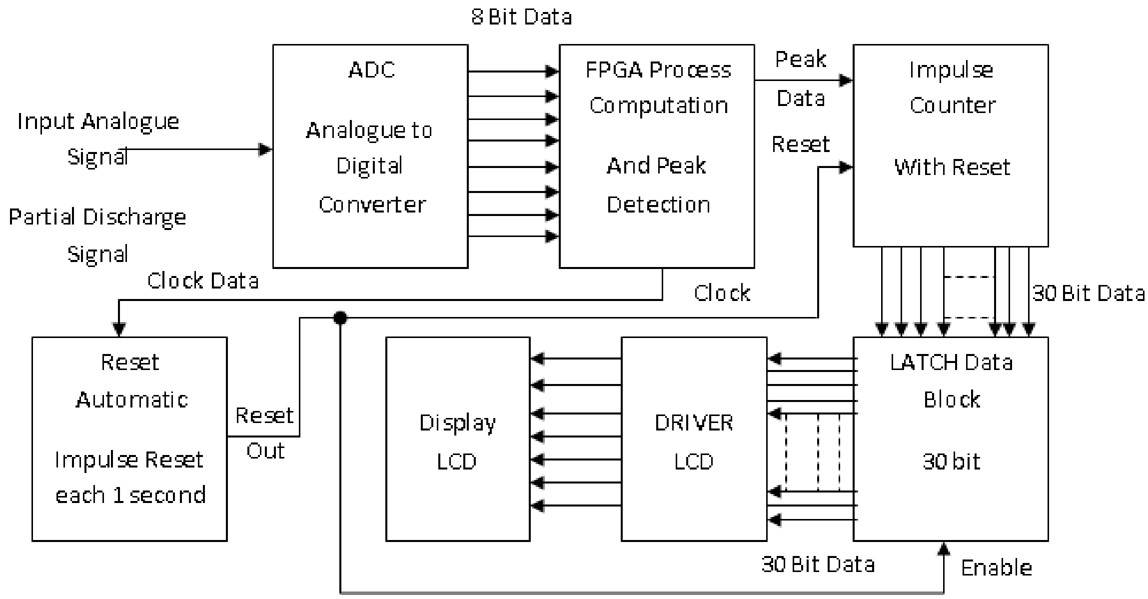


Fig. 2 All Schematic Diagram of Block Diagram Partial Discharge Detection using FPGA

The function of ADC is to convert analogue signals to digital signals by sampling time, and digitize signal. FPGA with ADC is used as the real board integrates these two components. The purpose of the FPGA and the ADC converter is for counting the amount of PD signals from ADC signal in the FPGA and then perform the computation of the real time data using intelligence algorithm in VHDL Programming. Fig. 3 shows the input PD signals.

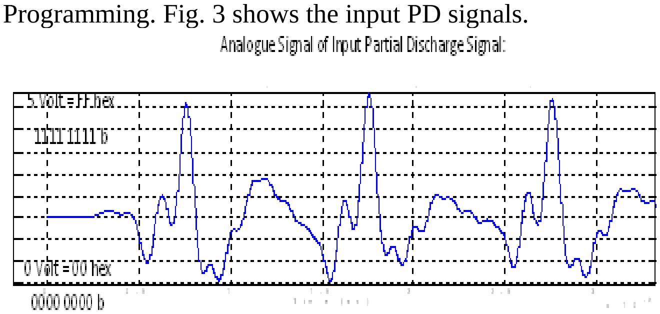


Fig. 3 Input Data Analogue from ADC

A.1. *Block Diagram ADC:*

Fig. 4 shows the block diagram data ADC.

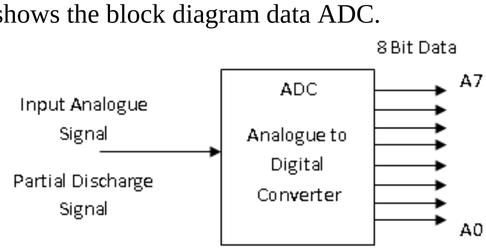


Fig. 4 Block Diagram Data ADC

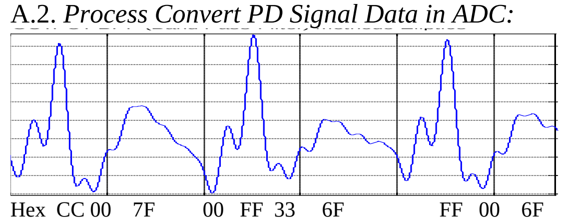
Fig. 5 shows the output data in ADC block. There are 256 levels to convert Analogue Data to Digital Data when process conversion data from 0 Volt to 5 Volt.

OUTPUT Data in ADC Block:

	A7	A6	A5	A4	A3	A2	A1	A0
(5 Volt) FF =	1	1	1	1	1	1	1	1
	...	...	...	...	...	...	...	...
	...	...	...	...	...	...	...	...
(0 Volt) FF =	0	0	0	0	0	0	0	0

Fig. 5 Output Data in ADC Block

A.2. *Process Convert PD Signal Data in ADC:*



Data Convert: 1 Volt = 33 hex 2 Volt = 66 hex
3 Volt = 99 hex 4 Volt = CC hex 5 Volt = FF hex.

Fig. 6 Output Data of ADC Block in Hexadecimal

Equation:

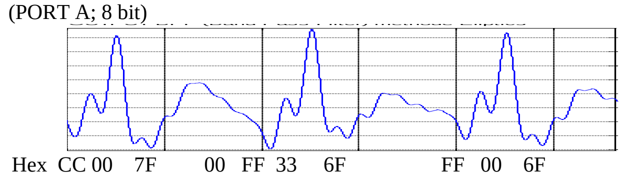
$$X\ Volt = \frac{x * 255}{5}\ dec = \text{convert to hex} \ \ldots.. \quad (1)$$

A.3. *Data input Partial Discharge in Binary Data:*

OUTPUT ADC (bin):

Fig. 7 shows the output data of ADC block in binary digital.

(PORT A; 8 bit)



Bin:

A_7	1	0	0	0	1	0	0	1	0	0
A_6	1	0	1	0	1	0	1	1	0	1
A_5	0	0	1	0	1	1	1	1	0	1

A_4	0	0	1	0	1	1	0	1	0	0
A_3	1	0	1	0	1	0	1	1	0	1
A_2	1	0	1	0	1	0	1	1	0	1
A_1	0	0	1	0	1	1	1	1	0	1
A_0	0	0	1	0	1	1	1	1	0	1

Fig. 7 Output Data of ADC Block in Binary digital

A.4. *Design ADC and PEAK Detection in FPGA:*

The function of this peak detector is for detect peak signals PD from sensor. In this simulation the peak detector is designed to have a 2.8 V = 8F hex threshold voltage. It means that if the input signal is more than 2.8 V or 8F hex, the output of the peak detector is logic 1 or 5 V and if input signal is less than 2.8 V or 8F hex, the output peak detector is logic 0 or 0 V. Detail of simulation model of Peak detector is shown in Fig.8.

A.5. *Block Diagram Simulation Model FPGA for ADC and PEAK Detection:*

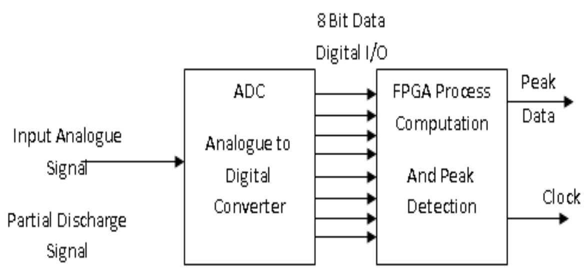


Fig. 8 Simulation Model FPGA of ADC and PEAK Detector using VHDL Programming

Comparator :

(Threshold = 8F hex = 2.803 Volt)

Threshold is designed in value 2.803 Volt or 8F hex to detect PD signals in peak detector block. Output of peak detector is logic high (logic 1=5V), if the input peak detector block is more than 8F hex or if input ADC block is more than 2.803 Volt. Output of peak detector is logic low (logic 0=0V), if the input peak detector block is less than 8F hex or if input ADC block is less than 2.803 Volt.

A.6. *Design Threshold for ADC and Peak Detector Block:*

Design Threshold for Analogue Signal of Input Partial Discharge Signal:

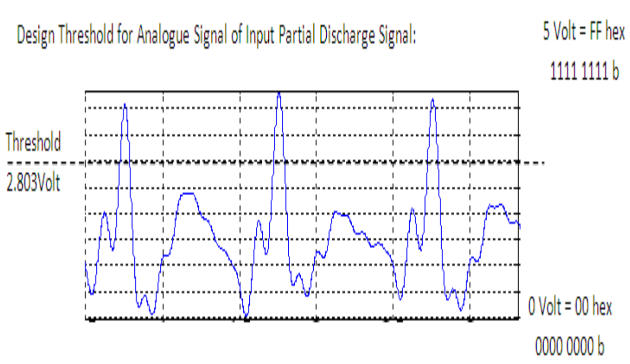


Fig. 9 Design Threshold for Input Data Analogue from ADC

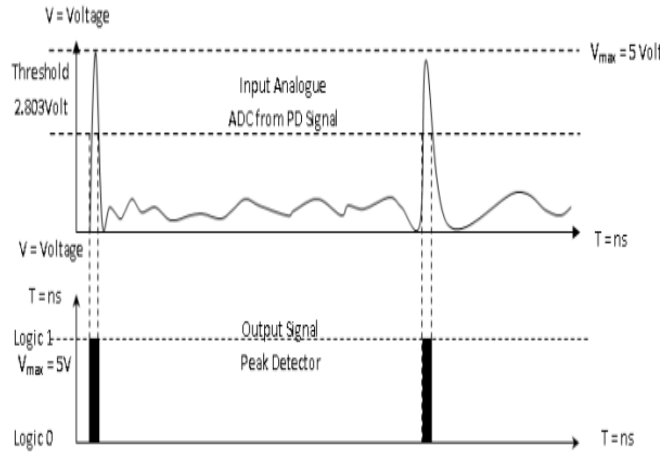


Fig.10. Design Threshold and Process Peak Detection

Fig. 9 shows the design threshold for input data analogue of ADC block in peak detector. Fig.10. shows the design threshold and output data of peak detector.

A.7. *Comparator between design VHDL and Verilog Programming for ADC and PEAK Detection block in FPGA:*

A.7.1. VHDL Programming:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity ADCandPEAK is
   Port ( CLOCK : in  STD_LOGIC;
          ADC : in  STD_LOGIC_VECTOR (7 downto 0);
          PEAK : out  STD_LOGIC);
end ADCandPEAK;

architecture Behavioral of ADCandPEAK is
signal PEAK_DETECT : std_logic := '0';
begin

process (CLOCK)
begin

  if (CLOCK'event and CLOCK ='1') then
    if (ADC > "10001111") then
      PEAK_DETECT <= '1';
    else
      PEAK_DETECT <= '0';
    end if;
  end if;
end process;
   PEAK <= PEAK_DETECT;
end Behavioral;
```

A.7.2. Verilog Programming

```
module ADCandPEAK(CLOCK, ADC, PEAK);
   input CLOCK;
   input [7:0] ADC;
   output PEAK;

  reg [0:0] PEAK = 1'b0;
  reg [7:0] threshold = 8'h8F; //or threshold = 8'b1000_1111;

   always @(posedge CLOCK)
    if (ADC > threshold)
```

```
    PEAK <= 1'b1;
  else
    PEAK <= 1'b0;

Endmodule
```

Listing programming A.71 shows the design VHDL programming for ADC and Peak detector block in FPGA technology. Listing programming A.72 shows the design Verilog programming for ADC and Peak detector block inn FPGA technology.

A.8. *Flow Chart Diagram for ADC and PEAK Detection Programming:*

Fig.10. shows the design flowchart diagram.

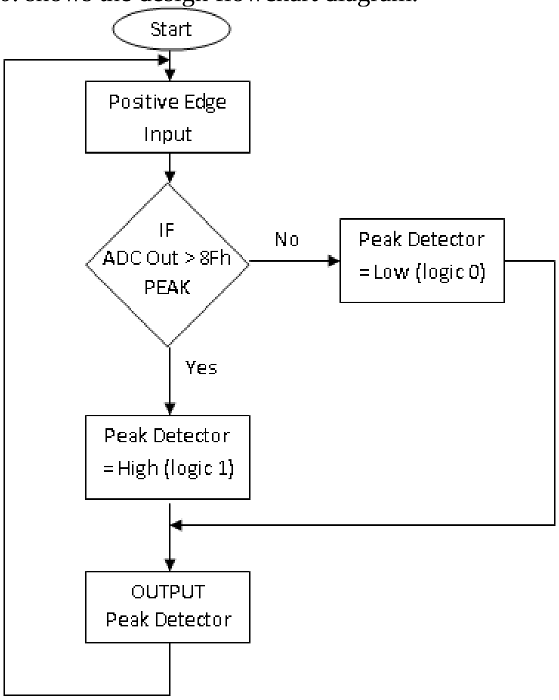


Fig.11. Design Flow Chart Diagram for ADC and Peak Detection Block in FPGA

Fig. 11 shows the design flow chart diagram for ADC and peak detector block in FPGA.

A.9. *Design Input Data Analogue ADC for Simulation PD signal in ADC and PEAK Detector of FPGA:*

Fig.12 shows the design input PD signal to FPGA board from ADC board before simulation VHDL using Xilinx ISE simulator.

Design input data before simulation as follow:

1. Input data 1st impulse from ADC is: 1110 1111 or EF hex (4.686 V).
2. Input data 2nd impulse from ADC is: 0000 0000 or 00 hex (0 V).
3. Input data 3rd impulse from ADC is: 1101 1111 or DF hex (4.372 V)
4. Input data 4th impulse from ADC is: 1011 1111 or BF hex (3.745 V)
5. Input data 5th impulse from ADC is: 0010 0000 or 20 hex (0.62 V).
6. Input data 6th impulse from ADC is: 0000 1000 or 08 hex (0.157 V).
7. Input data 7th impulse from ADC is: 0000 0010 or 02 hex (0.039 V).

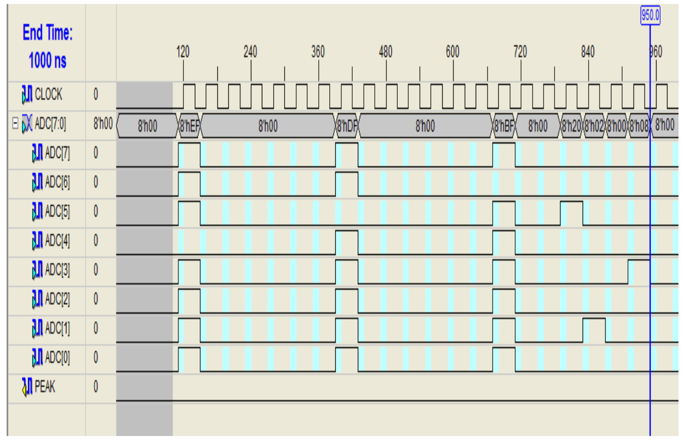


Fig.12. Design Input Data Analogue PD signal for ADC and Peak Detection Block

A.10. Design Platform FPGA for ADC and PEAK Detector Block:

Platform programming is VHDL (Very high speed integrated circuit Hardware Description Language) and Verilog programming.

Platform FPGA is:

1. FPGA Virtex 5 (ML501 Board)
2. Chipset FPGA is XC5VLX50
3. Package of Chipset is FF676

Design clock timing in FPGA Xilinx Virtex 5 is:

1. Clock High Time is : 20 ns
2. Clock Low Time is : 20 ns
3. Input setup Time is : 10 ns
4. Output Valid Delay is : 10 ns
5. Offset is : 100 ns
6. Initial Length of Test Bench is : 1000 ns

A.11. *Result Test Simulation for ADC and Peak Detector Block Programming:*

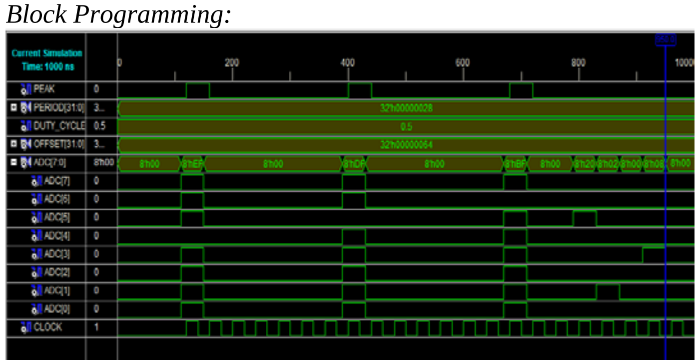


Fig.13. Simulation Model FPGA of ADC and Peak Detector Block using Test Bench Wave ISE Simulator from 0 ns until1000 ns

A.11.1 *Analysis Graphic:*

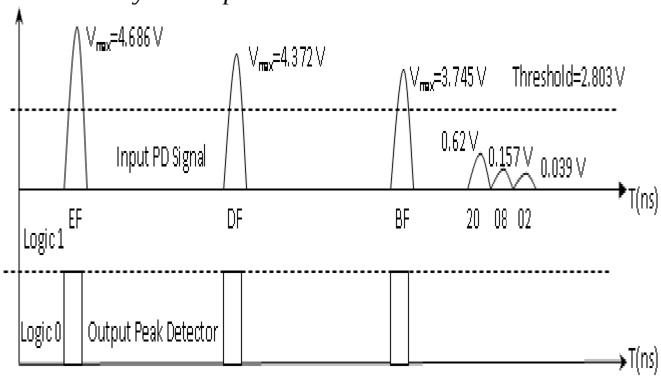


Fig.14. Analysis Simulation Model FPGA of ADC and Peak Detector Block Programming.

Result Test in fig.13. shows the peak detector can detect Peak of PD signal from input signal ADC. The Peak detector in this simulation is designed to have a 2.803 V = 8F hex threshold voltage. It means that if the input signal is more than 2.803 V or 8F hex, the output of the peak detector is logic 1 or 5 V and if input signal is less than 2.803 V or 8F hex, the output peak detector is logic 0 or 0 V. Detail of simulation model result of Peak detector is shown in Fig.14.

A.11.2 *Conclusion of the Simulation:*
This ADC and PEAK Detection Block has been successful to be running in FPGA Programming.

B. Block Counter and Reset :

B.1. *Design Counter and Reset Block:*
The purpose of the Counter and Reset Block is for counting the amount of PD signals from ADC signal and Peak detection Block in the FPGA and then perform the computation of the real time data using 30 bit digital Output data in VHDL Programming. So it means counter will run up counter from 0 to 1,073,741,824 counting or 0000 0000 hex to 3FFF FFFF hex counting. Counter will return back to 0 if the reset of counter is active. In this VHDL programming, counter is designed using reset active high (type negative edge reset) for Up Counter in FPGA. Fig.15. shows the input data analogue from ADC.

Digital Signal of Input Counter and Reset Block in FPGA:

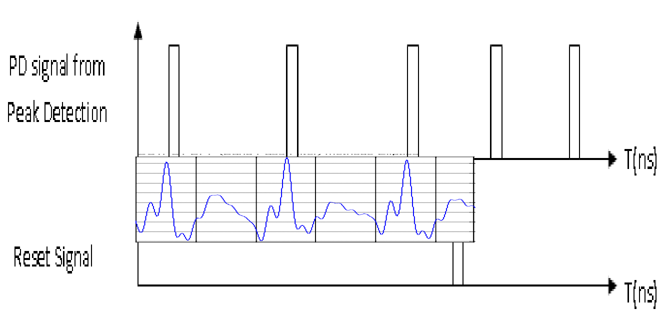


Fig.15. Input Data Analogue from ADC

B.2. *Block Diagram:*

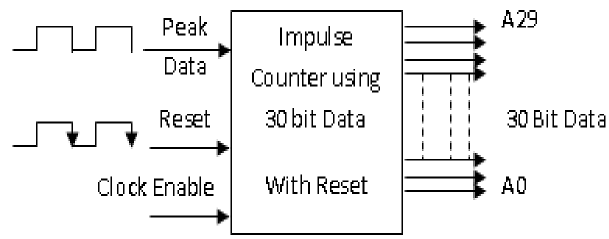


Fig.16. Block Diagram Design for 30 bit Counter and Reset Block in FPGA

Fig.16. shows the design 30 bit up counter with reset in FPGA.

OUTPUT Data in Counter and Reset Block:

	A29	A28	A27.....	A3	A2	A1	A0
3FFF FFFF =	1	1	1	1	1	1	1
	--------	--------	--------	--------	--------	--------	--------
	--------	--------	--------	--------	--------	--------	--------
0000 0000 =	0	0	0	0	0	0	0

There are 1,073,741,824 levels counting to count Digital PD signal Data from Peak detector when process counting data from 0000 0000 hex to 3FFF FFFF hex.

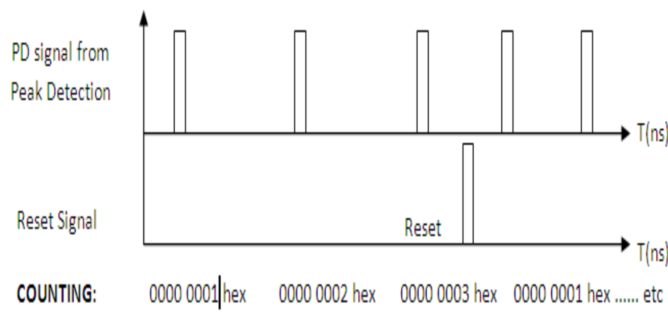


Fig.17. Block Diagram Design for 30 bit Counter and Reset Block in FPGA

Fig.17 shows desire result from design counter with reset block programming. The desire result have to show the output up counter increase when there is impulse signal, and the output up counter must be zero when the reset signal is active.

B.3. *Flow Chart Diagram for Counter and Reset Block Programming:*

Fig.18. shows the design flowchart diagram of Counter and Reset Block in FPGA. The first time program of counter is setting to positive edge input. The second step of the program is select data input, if the input reset data is active or logic high then the output counter must be reset to zero value. If the input reset data is not active or logic low, the program will continue the next step. The third step of the program is select input data of CE (chip enable). If the CE is given data active or logic high then the output data counter must be increase data by 1. If the CE is not active then data output counter must be the same with old data. So data output counter will be stop if CE is not active and the counter will run again after the input CE is active again.

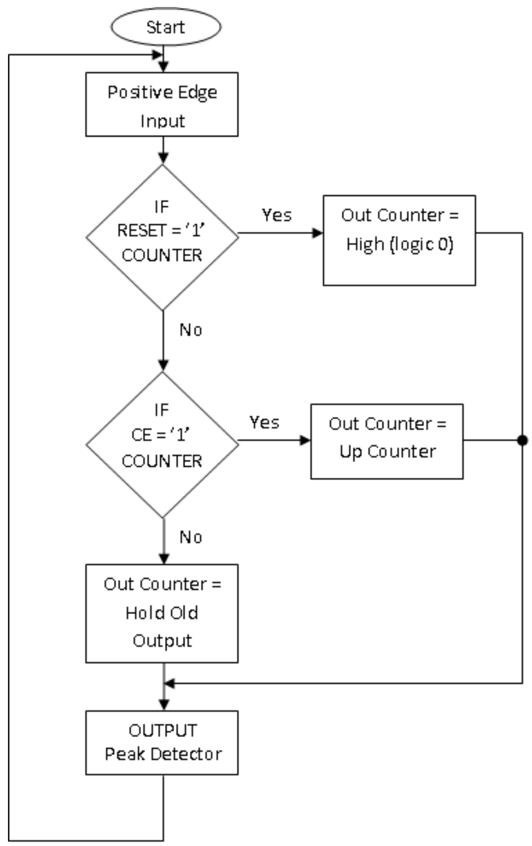


Fig.18. Design Flow Chart Diagram for Counter and Reset Block in FPGA

B.4. *Result Test Simulation for Counter and Reset Block Programming:*

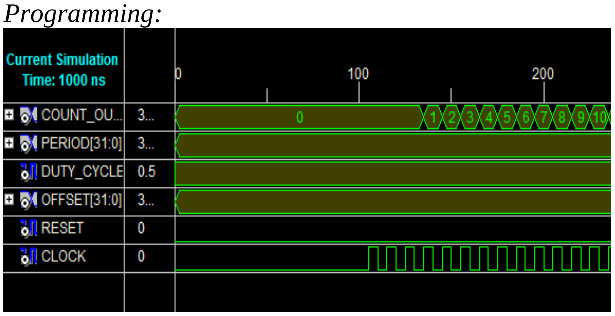


Fig.19. Simulation Model FPGA of Counter and Reset Block using Test Bench Wave ISE Simulator from 0 ns until 230 ns

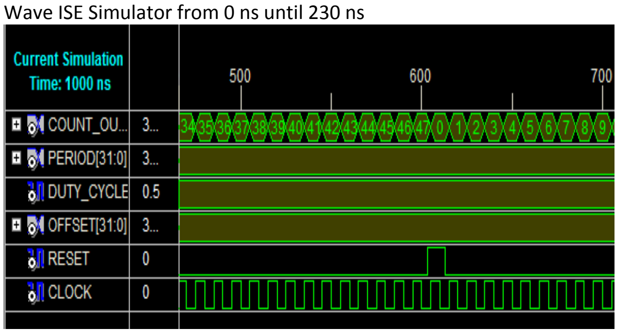


Fig.20. Simulation Model FPGA of Counter and Reset Block using Test Bench Wave ISE Simulator from 500 ns until 700 ns

B.4.1. *Analysis Graphic:*

Fig.20 and 21 shows the up counter is running from 0 to 46 hex when Reset is not active and Chip Enable is active. Up counter is running depend of amount impulse Peak Detector from input Counter and Reset Block. If there is impulse reset is active in 600 ns, the counter is return back to 0 and do up counting again.

B.4.2. *Conclusion of the Simulation:*

The Up Counter and Reset Block has been successful to synthesis, compile, simulate and run in FPGA Programming.

C. Combination ADC-Peak Detection and Counter-Reset Block

C.1. Design Peak Detector and Up Counter Block:

The counter will reset each 1µs, and the data output will be hold by a latch for display purpose. The data will be updated to display each 0.5µs or 500ns in FPGA. For constant impulse signal rate, there will be 10^8 Impulse in 1 second if there is 1 impulse in each 10 ns. In real system data will be updated to display each 1second in FPGA.

C.2. Block Diagram of Peak Detector and Counter:

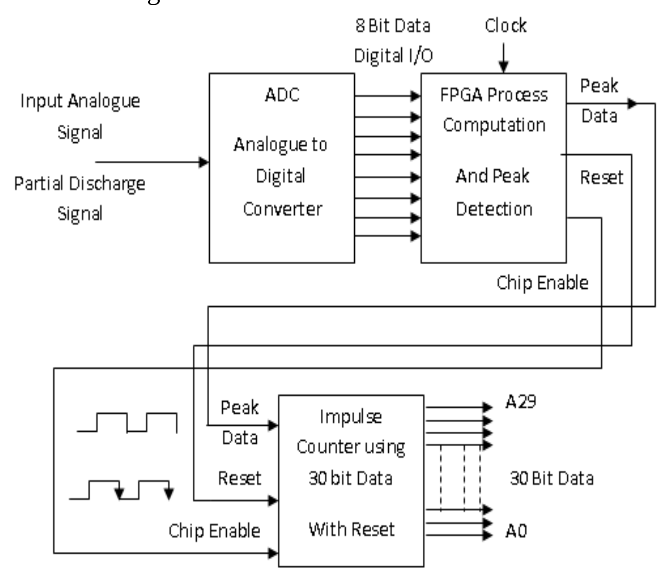


Fig.21.Simulation Model FPGA of Peak Detector and Up Counter Block using Test Bench Wave ISE Simulator

Fig.21. shows the simulation model FPGA of peak detector and up counter with reset block.

Design clock timing in FPGA Xilinx Virtex 5 for simulation model FPGA of peak detector and up counter with reset block is:

1. Clock High Time is : 5 ns
2. Clock Low Time is : 5 ns
3. Input setup Time is : 2 ns
4. Output Valid Delay is : 2 ns
5. Offset is : 100 ns
6. Initial Length of Test Bench is : 1000 ns

C.3. *Flow Chart Diagram for Combination ADC with Peak Detector Block and Counter with Reset Block Programming:*

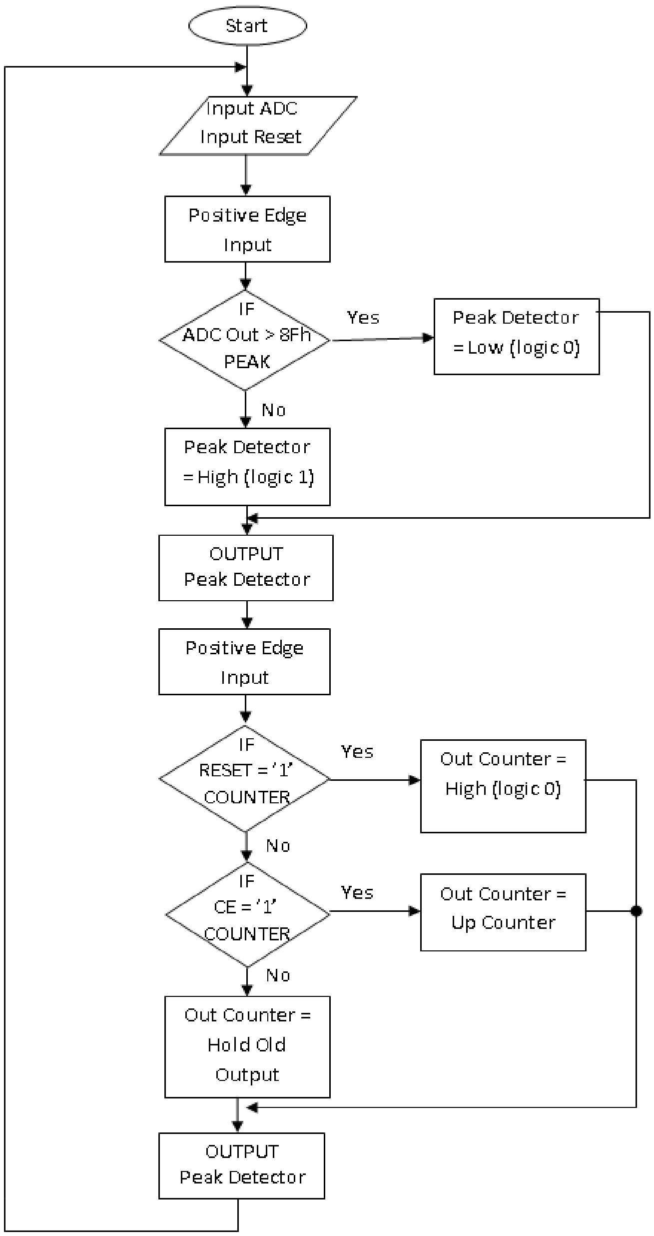


Fig.22.Simulation Combination Peak Detector Block and Counter Block

Fig.22. shows the design flowchart diagram of Combination ADC with Peak Detector Block and Counter with Reset Block in FPGA.

III. SIMULATION RESULT

A. *Test Simulation FPGA using Test Bench* Wave for ADC and PEAK Detection Programming:

A.1. Simulation Result Graph:

Fig. 23 shows the result test simulation model of ADC and Peak Detector block programming. Table.1 shows the data result of simulation test of ADC and Peak Detector block programming. Fig.24 shows the analysis graphic of simulation ADC and Peak Detector block programming.

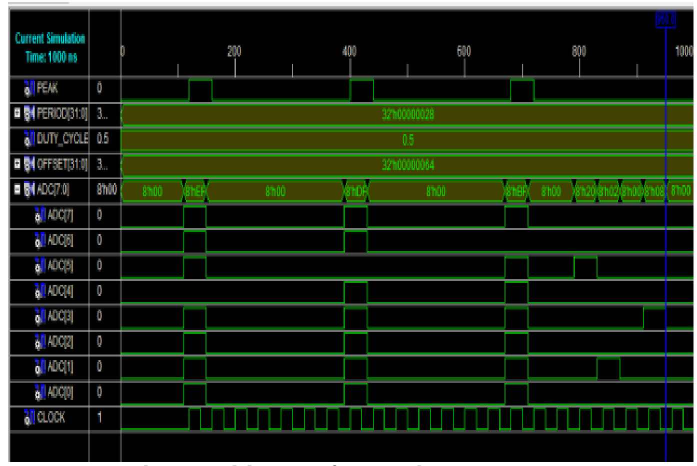


Fig.23. Simulation Model FPGA of ADC and PEAK Detector using Test Bench Wave ISE Simulator

A.2. Result Test:

Table 1. Data Result Test Peak Detector

Input Data From ADC Threshold = 8F hex = 2.803 Volt

No.	Data Binary	Data Hex	Data in Voltage	Output Peak
01.	1110 1111	EF	4.686 V	high (logic 1)
02.	0000 0000	00	0 V	low (logic 0)
03.	1101 1111	DF	4.372 V	high (logic 1)
04.	1011 1111	BF	3.745 V	high (logic 1)
05.	0010 0000	20	0.62 V	low (logic 0)
06.	0000 1000	08	0.157 V	low (logic 0)
07.	0000 0010	02	0.039 V	low (logic 0)

The data experiment lab of simulation VHDL programming shows output peak detection is logic high when the input voltage more than 2.803 volt.

A.3. Analysis Graphic:

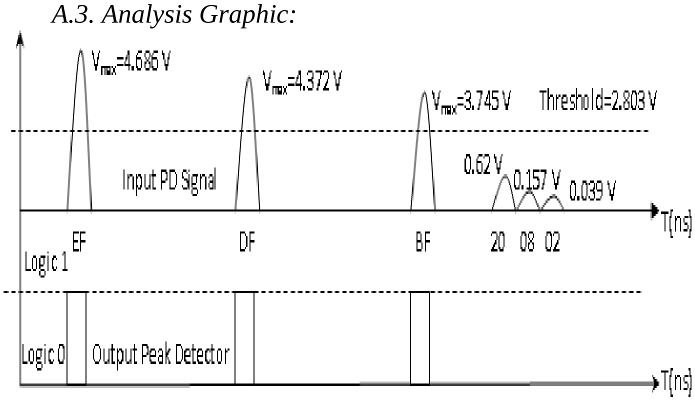


Fig.24. Analysis Graphic of Simulation Model FPGA for ADC and PEAK Detector Block

B. Simulation FPGA for Combination ADC with Peak Detector Block and Counter with Reset Block Programming

B.1. Simulation Result:

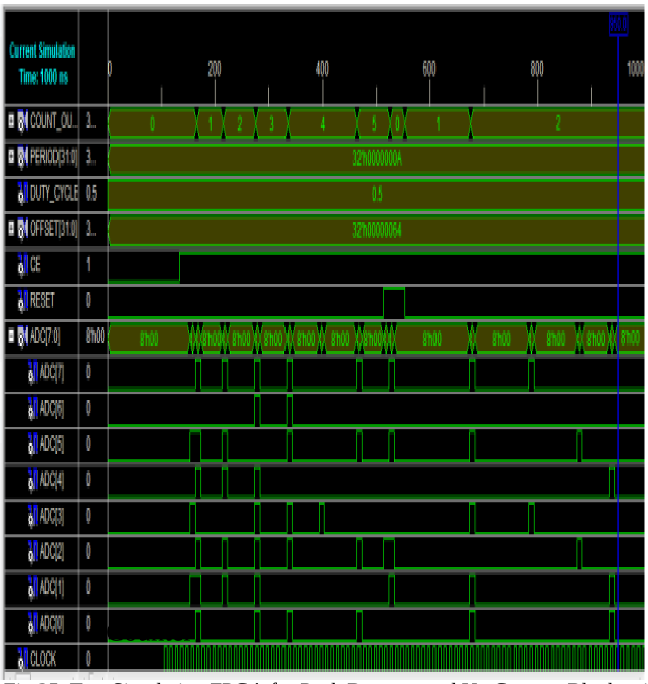


Fig.25. Test Simulation FPGA for Peak Detector and Up Counter Block using Test Bench Wave

B.2. Analysis Graphic:

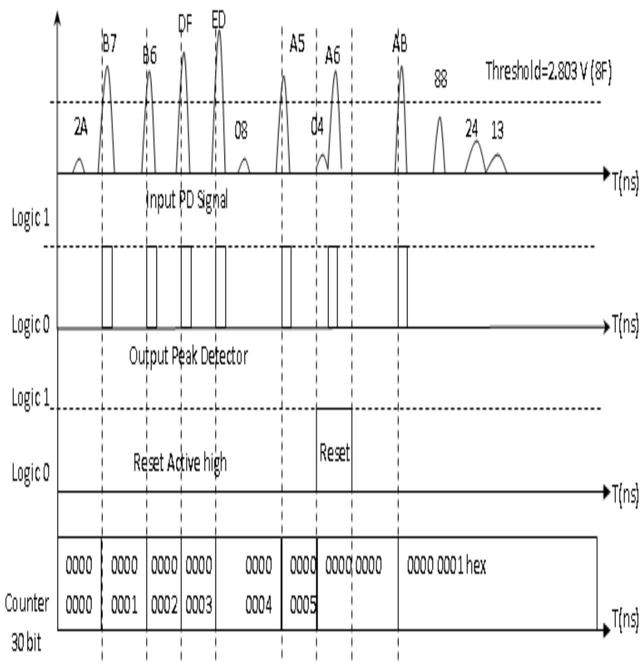


Fig.26. Analysis Graphic Signal for Peak Detector and Up Counter Block in Simulation FPGA

Fig.25 shows the result test of simulation combination ADC with peak detector block and counter with reset block programming in VHDL. Fig.26 shows the analysis graphic signal of combination ADC with peak detector block and counter with reset block. Fig.25 and 26 shows the up counter is running from 0 to 5 hex when Reset is not active and Chip Enable is active. Up counter is running depend of amount impulse Peak Detector from input Counter and Reset Block. If there is impulse reset is active in 500 ns, the counter is return back to 0 and do up counting again.

The up counter is counting when there is input analogue PD signal from ADC that more than threshold line 2.803 Volt or 8F hex. The up counter will return to zero (0) again if reset is active (the reset is active high).

V. CONCLUSION

Result Test show that Output Peak Detector can detect Peak signal from input signal ADC. The Peak detector in this simulation is designed to have a 2.803 V = 8F hex threshold voltage. It means that if the input signal is more than 2.803 V or 8F hex, the output of the peak detector is logic 1 or 5 V and if input signal is less than 2.803 V or 8F hex, the output peak detector is logic 0 or 0 V. This ADC and PEAK Detection Block has been successful to be running in FPGA Programming.

The ADC-Peak Detector and Up Counter-Reset Block has been successful to synthesis, compile, simulate and run in FPGA Programming. Combination ADC-Peak-Counter can work successfully.

VII. REFERENCE

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